AMENDMENTS TO THE CLAIMS

1. (Reinstated, Original) A method for performing a layout beautification operation on an integrated circuit (IC) layout comprising a plurality of polygons, the method comprising applying a first action to a first portion of the IC layout responsive to determining that a first shape associated with the first action matches the first portion of the IC layout, the first shape comprising at least a first edge and a second edge related according to a defined property, the first shape being configured to match a first type of layout imperfection.

2. (Reinstated, Original) The method of Claim 1, wherein the first action comprises adjusting the first type of layout imperfection by a fixed amount.

3. (Reinstated, Original) The method of Claim 1, wherein the first type of layout imperfection covers a plurality of actual layout imperfections, each of the plurality of actual layout imperfections having a different set of actual properties, wherein the first action comprises making an adjustment according to the set of actual properties for each of the plurality of actual layout imperfections.

4. (Reinstated, Original) The method of Claim 1, wherein the first action comprises replacing the first type of layout imperfection with a second shape.

5. (Reinstated, Original) The method of Claim 1, wherein the first edge and the second edge are not contiguous.

6. (Reinstated, Original) The method of Claim 5, wherein the IC layout comprises a first layer and a second layer, the first edge being associated with the first layer, and the second edge being associated with the second layer.

7. (Reinstated, Original) The method of Claim 6, wherein the first layer comprises a gate layer, and wherein the second layer comprises a wire layer.

8. (Reinstated, Original) The method of Claim 1, wherein the defined property specifies a plurality of alternative relationships between the first edge and the second edge.

9. (Reinstated, Original) The method of Claim 1, the second edge being contiguous with and substantially perpendicular to the first edge, and wherein the first shape further comprises a third edge, the third edge being contiguous with and substantially perpendicular to the second edge, the third edge being substantially parallel to and side-by-side with the first edge.

10. (Reinstated, Original) The method of Claim 1, the second edge being contiguous with and substantially perpendicular to the first edge, and wherein the first shape further comprises:

a third edge, the third edge being contiguous with and substantially perpendicular to the second edge, wherein the third edge is not substantially side-by-side with the first edge;

a fourth edge, the fourth edge being contiguous with and substantially perpendicular to the third edge, wherein

the fourth edge is not substantially side-by-side with the second edge;

a fifth edge, the fifth edge being contiguous with and substantially perpendicular to the fourth edge, wherein the fifth edge is substantially parallel to and side-by-side with the third edge;

a sixth edge, the sixth edge being contiguous with and substantially perpendicular to the fifth edge, wherein the sixth edge is not substantially side-by-side with the fourth edge; and

a seventh edge, the seventh edge being contiguous with and substantially perpendicular to the sixth edge, the seventh edge being substantially parallel to and side-by-side with the first edge.

11. (Previously Amended) A method for performing a layout beautification operation on an integrated circuit (IC) layout comprising a plurality of polygons, the method comprising applying a first action to a first portion of the IC layout responsive to determining that a first shape associated with the first action matches the first portion of the IC layout,

the first shape comprising at least a first edge and a second edge related according to a defined property, the first shape being configured to match a first type of layout imperfection,

the second edge being contiguous with and substantially perpendicular to the first edge, and wherein the first shape further comprises:

a third edge, the third edge being contiguous with and substantially perpendicular to the second edge;

a fourth edge, the fourth edge being contiguous with and substantially perpendicular to the third edge; and

a fifth edge, the fifth edge being contiguous with and substantially perpendicular to the fourth edge, wherein none of the first edge, the second edge, the third edge, the fourth edge, and the fifth edge are substantially side-by-side with each other.

12. (Reinstated, Original) A method for correcting a plurality of layout imperfections in an integrated circuit (IC) layout, the method comprising:

defining a plurality of shapes, each of the plurality of shapes comprising at least a first edge and a second edge related according to at least one of a plurality of defined properties, each of the plurality of shapes matching at least one of the plurality of layout imperfections;

defining a plurality of actions to correct the plurality of layout imperfections, each of the plurality of actions being associated with at least one of the plurality of shapes; and

applying the plurality of actions to the IC layout responsive to the at least one of the plurality of shapes associated with each of the plurality of actions matching elements within the IC layout.

13. (Reinstated, Original) The method of Claim 12, the plurality of actions having a specified sequence, wherein any element within the IC layout to which one of the plurality of actions is applied is excluded from further applications of the plurality of actions.

14. (Reinstated, Original) The method of Claim 13, the specified sequence being determined according to a predefined ranking of layout imperfection criticality.

15. (Reinstated, Original) The method of Claim 12, the IC layout comprising a plurality of polygons, each of the plurality of polygons comprising a plurality of elements, wherein applying the plurality of actions to the IC layout comprises:

applying the plurality of actions to the plurality of elements included in a first polygon in the plurality of polygons in a specified sequence; and

restarting the specified sequence when one of the plurality of actions is applied to one of the elements of the IC layout included in the first polygon.

16. (Reinstated, Original) The method of Claim 12, wherein applying the plurality of actions to the IC layout comprises:

applying a first action to the IC layout responsive to the at least one of the plurality of shapes associated with the first action matching elements in the IC layout; and

applying a second action to the IC layout responsive to the at least one of the plurality of shapes associated with the second action matching elements in the IC layout.

17. (Reinstated, Original) The method of Claim 12, the IC layout comprising a plurality of polygons, wherein applying the plurality of actions to the IC layout comprises:

applying each of the plurality of actions to a first polygon in the plurality of polygons responsive to the at least one of the plurality of shapes associated with each of the plurality of actions matching elements in the first polygon; and

applying each of the plurality of actions to a second polygon in the plurality of polygons responsive to the at least one of the plurality of shapes associated with the plurality of actions matching elements in the second polygon.

18. (Reinstated, Original) The method of Claim 17, further comprising initializing a lookup table, the lookup table incorporating the plurality of actions.

19. (Reinstated, Original) A system for performing layout beautification on an integrated circuit (IC) layout data file, the system comprising:

an input data manager for loading the IC layout data file into the system;

a layout beautification engine for applying a plurality of corrective actions to the IC layout data file responsive to at least one of a plurality of shapes associated with each of the plurality of corrective actions matching elements in the IC layout data file, wherein each of the plurality of shapes comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties; and

an output data manager for generating an output data file.

20. (Reinstated, Original) The system of Claim 19, wherein the IC layout data file comprises a fractured data file, and wherein loading the IC layout data file into the system comprises reassembling a plurality of layout primitives into a plurality of polygons.

21. (Reinstated, Original) The system of Claim 19, the IC layout data file having a first data file format, wherein loading the IC layout data file into the system comprises converting the first data file format into a second data file format, the layout beautification engine being configured to operate on the second data file format.

22. (Reinstated, Original) The system of Claim 21, wherein generating the output data file comprises converting the second data file format into a third data file format.

23. (Reinstated, Original) The system of Claim 19, wherein the layout beautification engine comprises a lookup table incorporating the plurality of corrective actions.

24. (Reinstated, Previously Amended) The system of Claim 19 further comprising a network connection to a remote storage location, wherein the remote storage location stores at least one of the IC layout data file and the plurality of corrective actions.

25. (Reinstated, Previously Amended) The system of Claim ~~25~~ 24, wherein the plurality of corrective actions are incorporated in a lookup table.

26. (Reinstated, Previously Amended) A system for performing layout beautification on an integrated circuit (IC) layout data file, the system comprising:

means for loading the IC layout data file into the system;

means for applying a plurality of corrective actions to the IC layout data file responsive to at least one of a

plurality of shapes associated with each of the plurality of corrective actions matching elements in the IC layout data file, wherein each of the plurality of shapes comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties; and

means for generating an output data file.

27. (Reinstated, Previously Amended) The system of Claim 26, the IC layout data file comprising a plurality of layers, wherein the means for loading the IC layout data file into the system comprises means for selecting at least one of the plurality of layers.

28. (Reinstated, Previously Amended) The system of Claim 26, the IC layout data file having a first data file format, wherein the means for loading the IC layout data file into the system comprises means for converting the first data file format into a second data file format, wherein the means for applying a plurality of corrective actions to the IC layout data file operates on the second data file format.

29. (Reinstated, Previously Amended) The system of Claim 28, wherein the means for generating the output data file comprises means for converting the second data file format into a third data file format.

30. (Reinstated, Previously Amended) The system of Claim 26, wherein the means for generating the output data file further comprises means for allowing a user to select the third data file format from a plurality of data file formats.

31. (Reinstated, Previously Amended) The system of Claim 26 further comprising means for accessing a remote storage location, wherein the remote storage location stores at least one of the IC layout data file and the plurality of corrective actions.

32. (Reinstated, Previously Amended) A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property; and

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features.

33. (Previously Amended) A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property; and

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and

a third set of instructions for defining the first shape according to a set of user inputs.

34. (Reinstated, Previously Amended) The software program of Claim 32, wherein the first layout beautification action comprises modifying each of the first set of matching features by a fixed amount.

35. (Reinstated, Previously Amended) The software program of Claim 32, wherein each of the first set of matching features can comprise a different characteristic, and wherein the first layout beautification action comprises performing a modification on each of the first set of matching features, the modification being based on the different characteristic of each of the first set of matching features.

36. (Reinstated, Previously Amended) The software program of Claim 32, wherein the first layout beautification action comprises replacing each of the first set of matching features with a second shape.

37. (Previously Amended) A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout

features, the first shape comprising at least a first edge and a second edge related according to a first property; and

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and

a third set of instructions for loading the first shape from across a network.

38. (Previously Amended) A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property; and

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and

a third set of instructions for defining the first layout beautification action according to a set of user inputs.

39. (Previously Amended) A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property; and

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and

a third set of instructions for loading the first action from across a network.

40. (Previously Amended) A software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program comprising:

a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property; and

a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features; and

a third set of instructions for comparing a second shape to the plurality of features in each of the plurality of polygons to identify a second set of matching layout features, the second shape comprising at least a third edge and a fourth edge related according to a second property; and

a fourth set of instructions for performing a second layout beautification action on the second set of matching layout features.

41. (Previously Amended) The software program of Claim 40, wherein the first set of instructions and the second set of instructions are completely executed before the third set of instructions and the fourth set of instructions.

42. (Previously Amended) The software program of Claim 40, wherein the first set of instructions and the second set of instructions are executed concurrently, and wherein comparing the first shape to a selected one of the plurality of features in each of the plurality of polygons is performed before comparing the second shape to the selected one of the plurality of features in each of the plurality of polygons.

43. (Previously Amended) The software program of Claim 40, wherein first action and the second action are incorporated in a lookup table.

44. (Reinstated, Previously Amended) An apparatus for reducing output data size in an input layout by beautifying the input layout, the apparatus comprising:

means for identifying a shape pattern in the input layout, wherein the shape pattern comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties; and

means for replacing the identified shape pattern with an alternative configuration, the alternative configuration reducing data volume.

45. (Reinstated, Previously Amended) The apparatus of Claim 44, wherein the alternative configuration provides one of an absolute correction, an adaptive correction, and a replacement correction.

46. (Reinstated, Previously Amended) A method of providing corrective actions to a layout based on shape analysis, the method comprising:

identifying shape patterns on the layout, wherein each shape pattern comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties; and

modifying the layout according to corrective actions associated with the identified shape patterns, thereby removing at least one layout imperfection, wherein the corrective actions include at least one of:

performing a first operation using a fixed value associated with an existing layout parameter of an identified shape pattern;

performing a second operation that is a function of an existing layout parameter of an identified shape pattern; and

performing a third operation that replaces an identified shape pattern.

47. (Reinstated, Previously Amended) The method of Claim 46, wherein performing the first operation includes matching a dimensional specification of a design rule and the existing layout parameter.

48. (Reinstated, Previously Amended) The method of Claim 46, wherein performing the first operation includes fixed biasing.

49. (Reinstated, Previously Amended) The method of Claim 46, wherein performing the second operation includes providing a corrective action proportional to the existing layout parameter.

50. (Reinstated, Previously Amended) The method of Claim 46, wherein performing the second operation includes at least one of proportional biasing and negative biasing.

51. (Reinstated, Previously Amended) A shape-based beautification method in a layout, the method comprising:

identifying a shape pattern on the layout; and

applying at least one of an absolute correction, an adaptive correction, and a replacement correction to the identified shape pattern, thereby removing at least one layout imperfection and reducing fracturing data volume in the layout.

52. (Reinstated, Previously Amended) The method of Claim 51, wherein the absolute correction includes matching a dimensional specification of a design rule and an existing layout parameter of the identified shape pattern.

53. (Reinstated, Previously Amended) The method of Claim 51, wherein the adaptive correction includes providing a corrective action proportional to the existing layout parameter.

54. (Reinstated, Previously Amended) The method of Claim 51, wherein the replacement correction replaces the identified shape pattern with a simplified shape pattern.